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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,863	01/10/2002	Chung-Liang Chang	TS01-603	8427
28112 759	90 11/26/2003		EXAMINER	
GEORGE O. S	SAILE & ASSOCIATE	CHEN, KIN CHAN		
28 DAVIS AVENUE POUGHKEEPSIE, NY 12603			ARTUNIT	PAPER NUMBER
100011111111111111111111111111111111111			1765	
			DATE MAR 6D- 11/26/200	2

Please find below and/or attached an Office communication concerning this application or proceeding.

	1	Applicati	on No.	Applicant(s)			
Office Action Summary		10/043,8		CHANG ET AL.			
		Examine		Art Unit			
		Kin-Chan		1765			
	The MAILING DATE of this communication			l '			
Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status							
1)[Responsive to communication(s) filed on	17 October 200	<u>3</u> .				
2a)⊠	This action is FINAL . 2b) This action is non-final.						
3)[3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
 4) ☐ Claim(s) 1-37 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-37 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement. 							
Application Papers							
9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. §§ 119 and 120 12)							
Attachment	(s) e of References Cited (PTO-892)		4) Interview Summary	(PTO-413) Paper No(s)			
2) Notice	e of Draftsperson's Patent Drawing Review (PTO-948 nation Disclosure Statement(s) (PTO-1449) Paper No			atent Application (PTO-152)			

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DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1-12, 17-32, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (US 6,251,774; hereinafter "Harada") as evidenced by Chang (US 5,643,407).

In a method of forming a dual damascene structure, Harada (col. 6, lines 17-34; col. 7, lines 15-17: Figs. 1A-1F) teaches providing a substrate with at least one point of electrical contact, a layer of IMD, at east one opening being aligned with the point of electrical contact; depositing a layer of first photoresist material over the surface of IMD, filling at least one opening created through the layer of IMD; removing the layer of first photoresist material form the surface of the layer of IMD, thereby removing the first photoresist from at least one opening created through the layer of IMD, creating at least one partial opening through the IMD; baking the substrate for a period of time by applying an elevated temperature in a gaseous environment and under pressure to the substrate. Significantly, Harada teaches using hot plate at a temperature of 150°C for 120 sec (col. 6, lines 26-27) and using hard baking or a combination of irradiation (col. 7, lines 15-16). This is significant because such as moisture in the openings would inherently be removed.

Harada teaches that a BARC may be deposited before depositing a layer of second photoresist over the surface of the layer of IMD. It is known in the art of

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semiconductor device fabrication that BARC is optionally applied under the photoresist to ensure that no light is reflected back from the chip surface into photoresist and to avoid exposure-disturbing. Therefore it can be omitted as instantly claimed invention. Without BARC, Harada teaches the method comprising depositing a layer of the second photoresist over the surface of the layer of IMD, thereby filling the at least one partial opening created through the layer of IMD and pattering and etching the layer of the second photoresist; creating an opening through the layer of the second photoresist that aligns with the at least one partial opening created through the layer of IMD, removing the layer of second photoresist from the at least one partial opening created through the layer of IMD.

As to dependent claims 2, 3, 20, and 23, Harada is not particular about the photoresist used in the process. Hence, it would have been obvious to one with ordinary skill in the art to use said photoresists because they are commonly used in the art of semiconductor device fabrication.

The above-cited claims differ from the prior art by specifying well-known features (such as using hot plate or furnace for baking in claims 4, 5, 24, 25; applying wet etch for creating an opening in IMD in claims 17 and 37) to the art of semiconductor device fabrication. A person having ordinary skill in the art) would have found it obvious to modify Harada by adding any of same well-known features to same in order to provide their art recognized advantages and produce an expected result.

The above-cited claims differ from the prior art by specifying various processing parameters (such as baking temperatures, pressure, and period of time in claims 6-8,

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12, 26-28, and 32). However, they are commonly determined by routine experiment. The process of conducting routine optimizations so as to produce an expected result is obvious to one of ordinary skill in the art. Hence, it is the examiner's position that a person having ordinary skill in the art at the time of the claimed invention would have found it obvious to modify Harada by performing routine experiments to obtain optimal result. Chang (col. 4, lines 45-48) is cited as evidence to show that baking semiconductor substrate is commonly performed in a nitrogen ambient at temperature about 250 °C to 350°C for between 20-40 minutes.

It is noted that applicant did not traverse the aforementioned conventionality (e.g., well-known features, obviousness), which have been stated in the office action (May 1, 2003).

2. Claims 13-16 and 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (US 6,251,774; hereinafter "Harada") as applied to claims 1-12, 17-32, and 37 above, and further in view of Chooi et al. (US 6,284,657; hereinafter "Chooi") or Chung et al. (US 6,017,817; hereinafter "Chung").

The discussion of modified Chooi from above is repeated here.

Harada teaches forming dual damascene structure, but does not detail the conventional damascene structure forming steps. Chooi or Chung is relied on only to show some conventional process steps such as depositing copper, filling the opening, removing the copper from the surface of the substrate using CMP. Because it is a conventional method to form dual damascene and because it is disclosed by Chooi or Chung, it would have been obvious to one with ordinary skill in the art to use same in

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the process of Harada in order to provide their art recognized advantages and produce an expected result.

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Response to Arguments

3. Applicant's arguments filed on October 17, 2003 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., due to adsorption or intrusion of moisture by the reacted DUV photoresist, the formation of a layer of scum photoresist has been taken place for low-k, non-oxide containing dielectric material; the baking step removes moisture from the dielectric and prevent the formation of scum photoresist) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant has argued that Harada does not teach baking the substrate. It is not persuasive. As has been stated in the office action, Harada teaches using hot plate at a temperature of 150°C for 120 sec (col. 6, lines 26-27) and using hard baking or a combination of irradiation (col. 7, lines 15-16).

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Conclusion

4. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kin-Chan Chen whose telephone number is (703) 305-

0222. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Nadine Norton can be reached on (703) 305-2667. The fax phone number

for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 308-2934.

NOVEMBER 21,2003

Kin-Chan Chen Primary Examiner

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